Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended): An apparatus for a compression architecture utilizing internal cache residing in main memory, the main memory comprising:

a compression cache to store a plurality of uncompressed data, wherein the compression cache is organized as a sectored cache that has associated tags that are on-die;

a compressed memory to store a plurality of compressed data; and

a compressed memory pointer table (CMPT) to store a plurality of pointers, the apparatus to assign a higher priority to compressed memory read operations in comparison to other operations.

Claim 2 (cancel)

Claim 3 (original): The apparatus of claim 1 wherein the compression cache has a plurality of associated tags that are incorporated within a memory interface coupled to the apparatus.

Claim 4 (original): The apparatus of claim 1 wherein the plurality of pointers are to the plurality of compressed data based on a plurality of cache block addresses.

Claim 5 (currently amended): The apparatus of claim 3, wherein the apparatus is coupled to [[a]] the memory interface that comprises:

a victim buffer to store at least one ~~the~~ entry that has been evicted from the compression cache;

a CMPT offset calculator to provide an offset relative to the start of the CMPT based on an actual address of the data being compressed.

Claim 6 (original): The apparatus of claim 5 wherein the memory interface is incorporated within a processor or a chipset.

Claim 7 (original): The apparatus of claim 6 wherein the apparatus is incorporated within a memory controller hub (MCH) of the chipset.

Claim 8 (original): The apparatus of claim 5 wherein the entry is evicted based on a first in first out (FIFO) protocol.

Claim 9 (currently amended): The apparatus of claim 1 wherein the CMPT is to store ~~stores~~ the plurality of pointers to the plurality of compressed data sequentially based on memory ~~address for which the data is compressed~~ addresses for the plurality of compressed data.

Claim 10 (currently amended): An apparatus for a memory interface comprising:

a first cache to store a plurality of tags for a compression cache;

a victim buffer to store at least one ~~the~~ entry that has been evicted from the compression cache;

an offset calculator to provide an offset relative to the start for a Compressed Memory Pointer Table (CMPT) based on an actual address of a data being compressed; and

a second cache to store a plurality of pointers for the CMPT, the apparatus to assign a higher priority to compressed memory read operations in comparison to other operations.

Claim 11 (original): The apparatus of claim 10 wherein the memory interface is incorporated within a processor or a chipset.

Claim 12 (original): The apparatus of claim 11 wherein the apparatus is incorporated within a memory controller hub (MCH) of the chipset.

Claim 13 (original): The apparatus of claim 10 wherein the entry is evicted based on a first in first out (FIFO) protocol.

Claim 14 (currently amended): A method for operating [[an]] a memory operation comprising:

receiving a memory address for the memory operation;

storing a plurality of compressed data in a main memory; and

performing a tag match between the memory address and a first cache storing a plurality of tags for a compressed memory in the main memory, assigning a higher priority to compressed memory read operations in comparison to other operations.

Claim 15 (currently amended): The method of claim 14 further comprising accessing a plurality of uncompressed data ~~access~~ from ~~the~~ a compression cache ~~is performed~~ if the tag match resulted in a hit.

Claim 16 (original): The method of claim 14 further comprising locating a pointer and subsequently finding a compressed memory location based at least in part on the pointer if the tag match resulted in a miss for the memory operation for a read miss.

Claim 17 (original): The method of claim 14 further comprising compressing the data and storing it in a compressed memory location for the memory operation for a write miss.

Claim 18 (currently amended): A system comprising:

a processor; and

a main memory, coupled to the processor, with [[a]]:

a compression cache to store a plurality of uncompressed data, wherein the compression cache is organized as a sectored cache that has associated tags that are on-die;

a compressed memory to store a plurality of compressed data; and

a compressed memory pointer table (CMPT) to store a plurality of pointers, and to assign a higher priority to compressed memory read operations in comparison to other operations.

Claim 19 (original): The system of claim 18 wherein the compression cache is a sectored cache.

Claim 20 (currently amended): The system of claim 18 wherein the compression cache has a plurality of associated tags that are incorporated within a memory interface ~~coupled to the apparatus~~.

Claim 21 (original): The system of claim 18 wherein the plurality of pointers are to the plurality of compressed data based on a plurality of cache block addresses.

Claim 22 (currently amended): A system comprising:

a processor; and

a memory interface, coupled to the processor, with [[a]]:

a first cache to store a plurality of tags for a compression cache;

a victim buffer to store at least one ~~the~~ entry that has been evicted from the compression cache;

an offset calculator to provide an offset relative to the start ~~for~~ of a Compressed Memory Pointer Table (CMPT) based on an actual address of a data being compressed; and

a second cache to store a plurality of pointers for the CMPT.

Claim 23 (original): The system of claim 22 wherein the memory interface is incorporated within a processor or a chipset.

Claim 24 (cancel)

Claim 25 (original): The system of claim 22 wherein the entry is evicted based on a first in first out (FIFO) protocol.

Claim 26 (currently amended): A system comprising:

a processor, coupled to a memory bridge, the memory bridge to comprise;

a first cache to store a plurality of tags for a compression cache;

a victim buffer to store at least one ~~the~~ entry that has been evicted from the compression cache;

an offset calculator to provide an offset relative to the start ~~for~~ of a Compressed Memory Pointer Table (CMPT) based on an actual address of a data that is ~~being~~ compressed; and

a second cache to store a plurality of pointers for the CMPT address; and

a main memory, coupled to the memory bridge, to comprise;

a compression cache to store a plurality of uncompressed data;

a compressed memory to store a plurality of compressed data; and

a compressed memory pointer table (CMPT) to store a plurality of pointers.

Claim 27 (original): The system of claim 26 wherein the compression cache is a sectored cache.

Claim 28 (original): The system of claim 26 wherein the compression cache has a plurality of associated tags that are incorporated within a memory interface coupled to the apparatus.

Claim 29 (original): The system of claim 26 wherein the plurality of pointers are to the plurality of compressed data based on a plurality of cache block addresses.